DPP - Daily Practice Problems

Name : Date :

Start Time : End Time :

PHYSICS 58

SYLLABUS : SEMICONDUCTOR ELECTRONICS-2 (Junction transistor, transistor action, characteristics of a transistor, transistor as an amplifier, logic gates)

Max. Marks : 112 **Time : 60 min.**

GENERAL INSTRUCTIONS

- The Daily Practice Problem Sheet contains 28 MCQ's. For each question only one option is correct. Darken the correct circle/ bubble in the Response Grid provided on each page.
- You have to evaluate your Response Grids yourself with the help of solution booklet.
- Each correct answer will get you 4 marks and 1 mark shall be deduced for each incorrect answer. No mark will be given/ deducted if no bubble is filled. Keep a timer in front of you and stop immediately at the end of 60 min.
- The sheet follows a particular syllabus. Do not attempt the sheet before you have completed your preparation for that syllabus. Refer syllabus sheet in the starting of the book for the syllabus of all the DPP sheets.
- After completing the sheet check your answers with the solution booklet and complete the Result Grid. Finally spend time to analyse your performance and revise the areas which emerge out as weak in your evaluation.

DIRECTIONS (Q.1-Q.20) : There are 20 multiple choice questions. Each] question has 4 choices (a), (b), (c) and (d), out of which **ONLY ONE** choice is correct.

Q.1 A NPN transistor conducts when
(a) both collector and emitter are positive with respect to the base
(b) collector is positive and emitter is negative with respect to the base
(c) collector is positive and emitter is at same potential as the base
(d) both collector and emitter are negative with respect to the base

Q.2 In the case of constants α and β of a transistor
(a) $\alpha = \beta$ (b) $\beta < 1, \alpha > 1$
(c) $\alpha = \beta^2$ (d) $\beta > 1, \alpha < 1$

Q.3 In an NPN transistor 10^{10} electrons enter the emitter in 10^{-6} s and 2% electrons recombine with holes in base, then α and β respectively are
(a) $\alpha = 0.98, \beta = 49$ (b) $\alpha = 49, \beta = 0.98$
(c) $\alpha = 0.49, \beta = 98$ (d) $\alpha = 98, \beta = 0.49$

Q.4 If l_1, l_2, l_3 are the lengths of the emitter, base and collector of a transistor then
(a) $l_1 = l_2 = l_3$ (b) $l_3 < l_2 > l_1$
(c) $l_3 < l_1 < l_2$ (d) $l_3 > l_1 > l_2$

Q.5 In an NPN transistor circuit, the collector current is 10 mA. If 90% of the electrons emitted reach the collector, the emitter current (i_E) and base current (i_B) are given by
(a) $i_E = -1\text{mA}, i_B = 9\text{mA}$ (b) $i_E = 9\text{mA}, i_B = -1\text{mA}$
(c) $i_E = 1\text{mA}, i_B = 11\text{mA}$ (d) $i_E = 11\text{mA}, i_B = 1\text{mA}$

RESPONSE GRID	1. ⓐⓑⓒⓓ	2. ⓐⓑⓒⓓ	3. ⓐⓑⓒⓓ	4. ⓐⓑⓒⓓ	5. ⓐⓑⓒⓓ

Space for Rough Work

Q.6 The transfer ratio of a transistor is 50. The input resistance of the transistor when used in the common-emitter configuration is 1 kΩ. The peak value for an A.C input voltage of 0.01 V peak is

(a) 100 μA (b) 0.01 mA

(c) 0.25 mA (d) 500 μA

Q.7 For transistor, the current amplification factor is 0.8. The transistor is connected in common emitter configuration. The change in the collector current when the base current changes by 6 mA is

(a) 6 mA (b) 4.8 mA

(c) 24 mA (d) 8 mA

Q.8 In NPN transistor the collector current is 10 mA. If 90% of electrons emitted reach the collector, then

(a) emitter current will be 9 mA

(b) emitter current will be 11.1 mA

(c) base current will be 0.1 mA

(d) base current will be 0.01 mA

Q.9 In a transistor in CE configuration, the ratio of power gain to voltage gain is

(a) α (b) β/α

(c) $\beta\alpha$ (d) β

Q.10 The following truth table corresponds to the logic gate

A	0	0	1	1
B	0	1	0	1
X	0	1	1	1

(a) NAND (b) OR

(c) AND (d) XOR

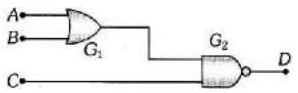
Q.11 The truth table shown in figure is for

A	0	0	1	1
B	0	1	0	1
Y	1	0	0	1

(a) XOR (b) AND

(c) XNOR (d) OR

Q.12 For the given combination of gates, if the logic states of inputs A, B, C are as follows $A = B = C = 0$ and $A = B = 1$, $C = 0$ then the logic states of output D are



(a) 0, 0 (b) 0, 1 (c) 1, 0 (d) 1, 1

Q.13 Correct statement for 'NOR' gate is that, it gives

(a) high output when both the inputs are low

(b) low output when both the inputs are low

(c) high output when both the inputs are high

(d) None of these

Q.14 A gate has the following truth table

P	1	1	0	0
Q	1	0	1	0
R	1	0	0	0

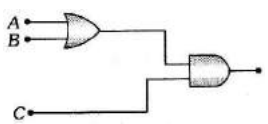
The gate is

(a) NOR (b) OR (c) NAND (d) AND

Q.15 What will be the input of A and B for the Boolean expression $\overline{(A+B)}.\overline{(A.B)} = 1$

(a) 0, 0 (b) 0, 1 (c) 1, 0 (d) 1, 1

Q.16 To get an output 1 from the circuit shown in the figure, the input can be



(a) $A = 0, B = 1, C = 0$ (b) $A = 1, B = 0, C = 0$

(c) $A = 1, B = 0, C = 1$ (d) $A = 1, B = 1, C = 0$

Q.17 The truth-table given below is for which gate?

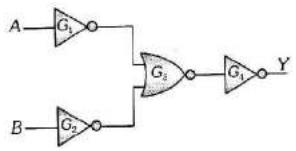
A	0	0	1	1
B	0	1	0	1
C	1	1	1	0

(a) XOR (b) OR (c) AND (d) NAND

RESPONSE GRID					
	6. ⓐⓑⓒⓓ	**7.** ⓐⓑⓒⓓ	**8.** ⓐⓑⓒⓓ	**9.** ⓐⓑⓒⓓ	**10.** ⓐⓑⓒⓓ
	11. ⓐⓑⓒⓓ	**12.** ⓐⓑⓒⓓ	**13.** ⓐⓑⓒⓓ	**14.** ⓐⓑⓒⓓ	**15.** ⓐⓑⓒⓓ
	16. ⓐⓑⓒⓓ	**17.** ⓐⓑⓒⓓ			

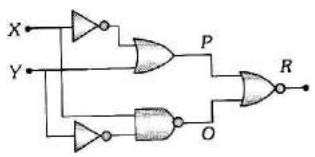
Space for Rough Work

Q.18 The combination of gates shown below produces



(a) AND gate (b) XOR gate
(c) NOR gate (d) NAND gate

Q.19 Figure gives a system of logic gates. From the study of truth table it can be found that to produce a high output (1) at *R*, we must have



(a) X = 0, Y = 1 (b) X = 1, Y = 1
(c) X = 1, Y = 0 (d) X = 0, Y = 0

Q.20 In the case of a common emitter transistor as/an amplifier, the ratio I_c/I_e is 0.96, then the current gain (β) of the amplifier is

(a) 6 (b) 48
(c) 24 (d) 12

DIRECTIONS (Q.21-Q.23) : In the following questions, more than one of the answers given are correct. Select the correct answers and mark it according to the following codes:

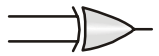
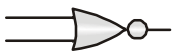
Codes :

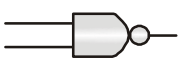
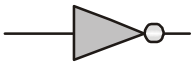
(a) 1, 2 and 3 are correct **(b)** 1 and 2 are correct
(c) 2 and 4 are correct **(d)** 1 and 3 are correct

Q.21 Which of the following are false?

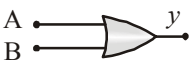
(1) Common base transistor is commonly used because current gain is maximum
(2) Common collector is commonly used because current gain is maximum
(3) Common emitter is the least used transistor
(4) Common emitter is commonly used because current gain is maximum

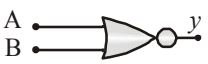
Q.22 Given below are symbols for some logic gates. The XOR gate and NOR gate are respectively

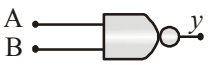
(1)  (2) 

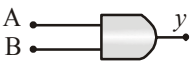
(3)  (4) 

Q.23 Given below are four logic gates symbol (figure). Those for OR, NOR and NAND are respectively

(1) 

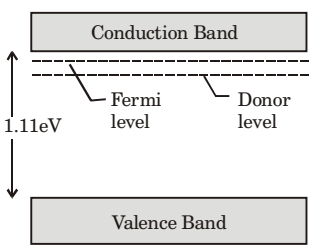
(2) 

(3) 

(4) 

DIRECTIONS (Q.24-Q.25) : Read the passage given below and answer the questions that follows :

Doping changes the fermi energy of a semiconductor. Consider silicon, with a gap of 1.11 eV between the top of the valence bond and the bottom of the conduction band. At 300K the Fermi level of the pure material is nearly at the mid-point of the gap. Suppose that silicon is doped with donor atoms, each of which has a state 0.15 eV below the bottom of the silicon conduction band, and suppose further that doping raises the Fermi level to 0.11 eV below the bottom of that band.



Q.24 For both pure and doped silicon, calculate the probability that a state at the bottom of the silicon conduction band is occupied? ($e^{4.524} = 70.38$)

(a) 5.20×10^{-2} (b) 1.40×10^{-2}
(c) 10.5×10^{-2} (d) 14×10^{-2}

Q.25 Calculate the probability that a donor state in the doped material is occupied? $e^{-1.547} = 0.212$

(a) 0.824 (b) 0.08
(c) 0.008 (d) 8.2

RESPONSE GRID					
	18. ⓐⓑⓒⓓ	**19.** ⓐⓑⓒⓓ	**20.** ⓐⓑⓒⓓ	**21.** ⓐⓑⓒⓓ	**22.** ⓐⓑⓒⓓ
	23. ⓐⓑⓒⓓ	**24.** ⓐⓑⓒⓓ	**25.** ⓐⓑⓒⓓ		

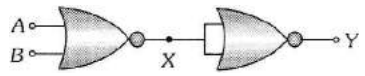
Space for Rough Work

DIRECTIONS (Q. 26-Q.28) : Each of these questions contains two statements: Statement-1 (Assertion) and Statement-2 (Reason). Each of these questions has four alternative choices, only one of which is the correct answer. You have to select the correct choice.

(a) Statement-1 is True, Statement-2 is True; Statement-2 is a correct explanation for Statement-1.
(b) Statement-1 is True, Statement-2 is True; Statement-2 is NOT a correct explanation for Statement-1.
(c) Statement -1 is False, Statement-2 is True.
(d) Statement -1 is True, Statement-2 is False.

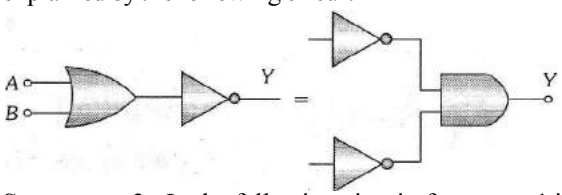
Q.26 Statement -1 : The logic gate NOT cannot be built by using diode.
Statement -2 : The output voltage and the input voltage of the diode have 180° phase difference.

Q.27 Statement -1 : The following circuit represents 'OR' gate

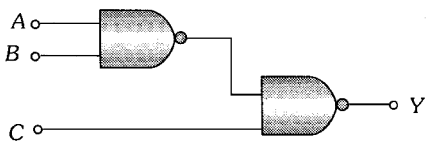


Statement-2 : For the above circuit $Y = \overline{X} = \overline{\overline{A+B}} = A+B$

Q.28 Statement -1 : De-morgan's theorem $\overline{A+B} = \overline{A}.\overline{B}$ may be explained by the following circuit



Statement -2 : In the following circuit, for output 1 inputs A,B,C are 1, 0, 1.



RESPONSE GRID	26. ⓐⓑⓒⓓ	27. ⓐⓑⓒⓓ	28. ⓐⓑⓒⓓ

DAILY PRACTICE PROBLEM SHEET 58 - PHYSICS			
Total Questions	28	Total Marks	112
Attempted		Correct	
Incorrect		Net Score	
Cut-off Score	26	Qualifying Score	46
Success Gap = Net Score – Qualifying Score			
Net Score = (Correct × 4) – (Incorrect × 1)			

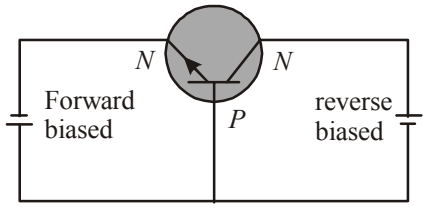
Space for Rough Work

DAILY PRACTICE PROBLEMS

PHYSICS SOLUTIONS

58

1. (b)



2. (d) α is the ratio of collector current and *emitter* current while β is the ratio of collector current and base current.

3. (a) Emitter current $I_e = \frac{Ne}{t} = \frac{10^{10} \times 1.6 \times 10^{-19}}{10^{-6}} = 1.6\,mA$

Base current $I_b = \frac{2}{100} \times 1.6 = 0.032\,mA$

But, $I_e = I_c + I_b$

$\therefore I_c = I_e - I_b = 1.6 - 0.032 = 1.568\,mA$

$\therefore \alpha = \frac{I_c}{I_e} = \frac{1.568}{1.6} = 0.98$ and $\beta = \frac{I_c}{I_b} = \frac{1.568}{0.032} = 49$

4. (d)

5. (d) $i_C = \frac{90}{100} \times i_E \Rightarrow 10 = 0.9 \times i_E \Rightarrow I_E = 11mA$

Also $i_E = i_B + i_C \Rightarrow i_B = 11 - 10 = 1mA$

6. (d) $\beta = 50, R = 1000\Omega, V_i = 0.01V$

$\beta = \frac{i_c}{i_b}$ and $i_b = \frac{V_i}{R_i} = \frac{0.01}{10^3} = 10^{-5}\,A$

Hence $i_c = 50 \times 10^{-5}\,A = 500\ \mu A$

7. (c) $\alpha = 0.8 \Rightarrow \beta = \frac{0.8}{(1-0.8)} = 4$

Also $\beta = \frac{\Delta i_c}{\Delta i_b} \Rightarrow \Delta i_c = \beta \times \Delta i_b = 4 \times 6 = 24mA$

8. (b) $i_e = i_b + i_c \Rightarrow i_c = i_e - i_b$

9. (b)

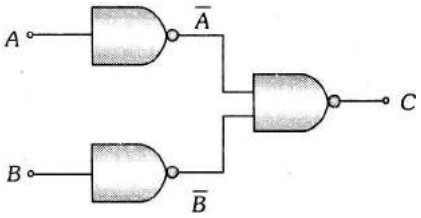
10. (d) For CE configuration voltage gain $= \beta \times R_L / R_i$

Power gain $= \beta^2 \times R_L / R_i \Rightarrow \frac{Power\ gain}{Voltage\ gain} = \beta$

11. (b) For 'OR' gate $X = A + B$

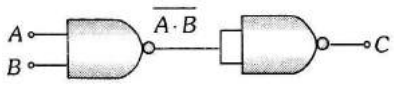
i.e. $0+0=0,\ 0+1=1, 1+0=1, 1+1=1$

12. (a)



$C = \overline{\bar{A}.\bar{B}} = \bar{\bar{A}} + \bar{\bar{B}} = A + B$ (De morgan's theorem)

Hence output C is equivalent to OR gate.



$C = \overline{AB}.\overline{AB} = \overline{\bar{A}.\bar{B}} + \overline{A.B} = AB + AB = AB$

In this case output C is equivalent to AND gate.

13. (c) For 'XNOR' gate $Y = \bar{A}\bar{B} + AB$

i.e. $\bar{0}\bar{0} + 0.0 = 1.1 + 0.0 = 1 + 0 = 1$

$\bar{0}\bar{1} + 0.1 = 1.0 + 0.1 = 0 + 0 = 0$

$\bar{1}\bar{0} + 1.0 = 0.1 + 1.0 = 0 + 0 = 0$

$\bar{1}\bar{1} + 1.1 = 0.0 + 1.1 = 0 + 1 = 1$

14. (d) The output D for the given combination

$D = \overline{(A+B).C} = \overline{(A+B)} + \bar{C}$

If $A = B = C = 0$ then

$D = \overline{(0+0)} + \bar{0} = \bar{0} + \bar{0} = 1 + 1 = 1$

If $A = B = 1, C = 0$ then

$D = \overline{(1+1)} + \bar{0} = \bar{1} + \bar{0} = 0 + 1 = 1$

15. (a) The Boolean expression for 'NOR' gate is $Y = \overline{A+B}$

i.e. if $A = B = 0$ (Low), $Y = \overline{0+0} = \bar{0} = 1$ (High)

16. (d) The Boolean expression for 'AND' gate is $R = P.Q$

$\Rightarrow 1.1 = 1, 1.0 = 0, 0.1 = 0, 0.0 = 0$

17. (a) The given Boolean expression can be written as

$Y = (\overline{A+B}).(\overline{A.B}) = (\bar{A}.\bar{B}).(\bar{A}+\bar{B}) = (\bar{A}\bar{A}).\bar{B} + \bar{A}(\bar{B}.\bar{B})$

$= \bar{A}.\bar{B} + \bar{A}\bar{B} = \bar{A}\bar{B}$

A	B	Y
0	0	1
1	0	0
0	1	0
1	1	0

18. (c) The Boolean expression for the given combination is output $Y = (A + B).C$

The truth table is

A	B	C	Y = (A + B).C
0	0	0	0
1	0	0	0
0	1	0	0
0	0	1	0
1	1	0	0
0	1	1	1
1	0	1	1
1	1	1	1

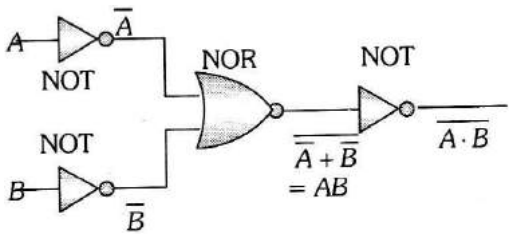
Hence A = 1, B = 0, C = 1

19. (d) For 'NAND' gate $C = \overline{A.B}$

i.e. $\overline{0.0} = \bar{0} = 1,\ \overline{0.1} = \bar{0} = 1$

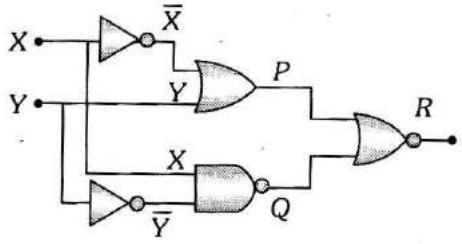
$$\overline{1.0} = \bar{0} = 1, \overline{1.1} = \bar{1} = 0$$

20. (d)



Hence option (d) is true.

21. (c)



True Table

X	Y	$\bar{X}$	$\bar{Y}$	$P = \bar{X} + Y$	$Q = \overline{X.\bar{Y}}$	$R = \overline{P+Q}$
0	1	1	0	1	1	0
1	1	0	0	1	1	0
1	0	0	1	0	0	1
0	0	1	1	1	1	0

Hence X = 1, Y = 0 gives output R = 1

22. (c) $\frac{I_c}{I_e} = 0.96$

$\Rightarrow \quad I_c = 0.96\, I_e$

But $I_e = I_c + I_b = 0.96\, I_e + I_b$

$\Rightarrow \quad I_b = 0.04\, I_e$

$\therefore$ Current gain, $\beta = \frac{I_c}{I_b} = \frac{0.96\, I_e}{0.04 I_e} = 24$

23. (a)

24. (b)

25. (a)

26. (b) The probability that a state with energy E is occupied is given by

$P(E) = \frac{1}{e^{(E-E_F)/kT} + 1}$, where E_F is the Fermi energy, T is the temperature on the Kelvin scale, and k is the Boltzmann constant. If energies are measured from the top of the valence band, then the energy associated with a state at the bottom of the conduction band is E = 1.11 eV. Furthermore, kT = $(8.62 \times 10^{-5}$ eV/K) (300K) = 0.02586 eV. For pure silicon, E_F = 0.555 eV and $(E - E_F)/kT = (0.555eV) / (0.02586eV) = 21.46$. Thus,

$$P(E) = \frac{1}{e^{21.46} + 1} = 4.79 \times 10^{-10}$$

For the doped semi-conductor,

$(E - E_F) / kT = (0.11\ eV) / (0.02586\ eV) = 4.254$

and $P(E) = \frac{1}{e^{4.254} + 1} = 1.40 \times 10^{-2}$.

27. **(a)** The energy of the donor state, relative to the top of the valence bond, is 1.11 eV – 0.15 eV = 0.96 eV. The Fermi energy is 1.11 eV – 0.11 eV = 1.00 eV. Hence,

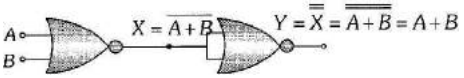
$(E - E_F)/kT = (0.96eV - 1.00eV)$

$/(0.02586eV) = -1.547$

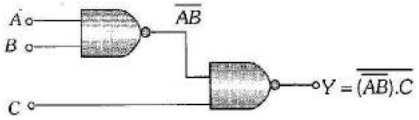
and $P(E) = \frac{1}{e^{-1.547} + 1} = 0.824$

28. (d) In diode the output is in same phase with the input therefore it cannot be used to built NOT gate.

29. (a) This is Boolean expression for 'OR' gate.



30. (d) Statement -1 is true but statement -2 is false.



If $A = 1, B = 0, C = 1$ then $Y = 0$